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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,302	12/12/2003	Junichi Tamura	OKI 402	7322

23995 7590 07/16/2007

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EXAMINER	
THOMAS, SHANE M	

ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
07/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/733,302	TAMURA, JUNICHI	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/12/2007 has been entered.

Information Disclosure Statement

As stated in the previous Office action filed 10/23/2006, the information disclosure statement filed 7/24/2006 has not been considered by the Examiner as a copy of the form PTO-1449 has not been included with Applicant's response. The cover page for the IDS as well as the references to be considered have been received by the Office, but the PTO-1449 which includes the reference listing has not been received. As such, the Examiner requests that the Applicant submit the form PTO-1449 in order for the IDS to be considered by the Examiner during the next response.

Claim Observations

Regarding claim 4, the claim states in limitation d) that the data in the first data storage section is addressed by the data rearrangement information. Other independent claims 1 and 8 regard the second data storage section being addressed by the data rearrangement information.

The Examiner merely points out this inconsistency; however, for the purposes of examination, the claim has been interpreted as claimed (data stored in the first data storage is addressed).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1,4, and 8, regarding step d), it is not clear whether Applicant is claiming that the "data is being addressed" by the data rearrangement information, wherein the data rearrangement information is stored in the second data storage section (wherein previously in step b) the data rearrangement information was claimed to be stored in the stack) or whether the "data being addressed" which itself is stored in the second data storage section, is being addressed by the data rearrangement information. For the purposes of examination, the Examiner has used the later interpretation and recommends amending limitation d) to read "addressing the data stored in the second data storage section by the data rearrangement information."

Claims 2,3,5-7,and 9-14 are rejected as being dependent upon a rejected base claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Durbin (U.S. Patent No. 4,611,310).

As per claims 1,4, and 8, Durbin teaches:

(a) storing data in a first data storage section (herein FDSS) - (memory loading procedure [4/3-52] into sort RAM 200);

b) storing data rearrangement information in a stack (stack RAM 334 - [10/1-40]);

c) reading the data stored in the FDSS and storing the data in a rearranged order in a second data storage second (herein second SDDS) (during an address rearrangement process, data in the FDSS is read in order to acquire the data to be rearranged [10/1-12] and the data comprising addresses of data record is stored in a rearranged order in Output RAM 300 - [10/14-16] and [10/37-40]) based on the data rearrangement information stored in the stack (stack data used during the address rearrangement process as taught in [10/23-34]);

d) addressing the data by the data rearrangement information in the second data storage section (since data rearrangement information stored in the stack RAM 334 are addresses of the Output RAM 300 [10/8-12], the data (e.g. addresses of the data records stored in the output RAM 300) are accessed by addressing the Output RAM 300 - [9/10-14].

Further regarding claims 4 and 8, a plurality of data may be stored in the FDSS as taught in the memory loading process [4/3-49]. Because the data rearrangement information stored in the stack RAM 334 further includes addresses of the FDSS in addition to addresses of the SDDS [10/1-10] in the same entry of the stack, the data in the FDDS may be accessed by the data rearrangement information as well.

As per claims 2,5, and 9, Durbin teaches that the data rearrangement information contains an address of the SDDS as discussed above and in [10/8-12].

As per claim 3, the Durbin teaches that the FDSS (sort RAM 200) may be a register (e.g. the single row of the sort RAM that corresponds to only the current entry being processed - [10/34-37] and figure 5B. The is considering each row of bits of the sort RAM to be a --register-- - [3/55-59]. Further, Durbin teaches that the SDSS is a RAM (output RAM 300 - [8/3-7]).

As per claim 6, Durbin teaches wherein the FDSS is a RAM (sort RAM - [3/55-56]) and the SDSS is a register (e.g. the single row entry of the output RAM 300 that contains the current entry that is to be read [9/10-16] or written [9/36-41].

As per claims 7 and 10, Durbin teaches wherein the FDSS and the second SDSS are RAMs - (sort RAM 200 and Output RAM 300).

As per claim 11, Durbin teaches that the reading and the storing are carried out by using an address conversion table (the stack RAM 334 converts the row of the sort RAM storing the necessary data to the corresponding row in the Output RAM 300 [10/4-10]) and a corresponding stack pointer (odd pass counter 338 selects an appropriate row/address of the stack RAM 334 - [10/10-12]).

As per claim 12, Durbin teaches calculating logic ADD operation of a read address (e.g. the address that at a time t_0 was stored in the Odd Pass counter 338 or Even Pass Counter 340 [11/31-33] before the counter is incremented at time t_1 by ADDing a logic "1" to increment the address) and an offset register (e.g. the flip-flop inherent to an up/down counter [9/67-68] that contains the logic value of "1" to increase/decrease the counter's value). Refer also to [10/28-30].

As per claim 13, Durbin teaches that the reading and the storing are carried out by using a register substituted for the stack pointer [11/15-20] and [11/35-38]. During one pass, the odd pass counter (e.g. the stack pointer) includes the address of the next location in which to write to the Stack RAM 334). When the first pass is over and the odd pass counter begins to decrement [10/28-30], a

--register-- containing an even counter is then used to begin a second pass where the process of incrementing the stack RAM address is repeated. Thus it can be seen that the register containing the even pass counter is substituted (functionally) for the stack pointer (odd pass counter) when the first and second pass are executing simultaneously [11/15-20].

As per claim 14, Durbin teaches the data stored in the address conversion table (stack RAM 334) includes byte write information as the address of the data record to be written to the Output RAM 300 from the stack RAM 334 is 8 bits in length as shown in figure 6A. Each entry row in the Stack RAM shows 8 bits (one byte) of information regarding which addresses of the Sort RAM 200 contain identical entries in the particular sub-keyfield [10/13-21] as well as 8 bits (one byte) of information regarding which address of the Output RAM 300 the data is to be written to (figure 6A, bits 256-263 and [10/9-12].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M. Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached on M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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